S/N To be assigned PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Ruuskanen	Serial No.:	To be assigned
Filed:	CONCURRENT HEREWITH	Docket No.:	796.422USWI
Title:	CONTROL OF PHASE LOCKED LOOP DURING CHANGE OF SYNCHRONISATION SOURCE		

CERTIFICATE UNDER 37 CFR 1.10
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By: Lee Thao
Name: Lee Thao

PRELIMINARY AMENDMENT

Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Please enter the following preliminary amendment into the above-referenced application.

ABSTRACT

Please insert the attached abstract into the application as the last page thereof.

CLAIMS

Please amend claims 1-6 as follows. A clean copy of the amended claims is included below. A marked up copy of the entire claim set is included in Appendix A.

1. (Amended) Method for controlling a phase locked loop during change of synchronisation source, in which method

- the synchronisation signal is changed from a first synchronisation to a second synchronisation signal,

- the phase difference between the said second synchronisation signal and a signal formed from the phase lock's oscillator is measured,

- the phase difference between the second synchronisation signal and the signal formed from the phase lock's oscillator is changed, if the measured phase difference is greater than a predetermined limit value, whereupon the phase difference between the said second synchronisation signal and the signal formed from the phase lock's oscillator is again measured,

- the phase locked loop's normal adjustment function is started, when the measured phase difference is less than or equal to the said limit value,

wherein

in response to the finding, that the said phase difference is less than or equal to the said limit value, the measured phase difference is set as the setting value for the phase difference for the normal adjustment function of the phase locked loop, whereupon the adjustment function is started.

2. (Amended) Method as defined in Claim 1, wherein phase transfer of the second synchronisation signal is carried out by preventing for a certain time access of the signal formed from the phase lock's oscillator to the component measuring the phase difference of the phase locked loop.

3. (Amended) Method as defined in Claim 2, wherein preventing takes place by cutting off the functional route of the signal formed from the oscillator to the component measuring the phase difference of the phase locked loop.

4. (Amended) Method as defined in Claim 2, wherein preventing takes place by cutting off the functional route of the second synchronisation signal to the component measuring the phase difference of the phase locked loop.

5. (Amended) Digital phase lock arrangement, which includes,

- selection components for selecting the desired synchronisation source from a set of at least two different synchronisation sources,

- a phase comparator, which has a first and a second input and which is used for generating an output signal dependent on the phase difference between the signals supplied to the inputs,

- controllers for forming a control word in response to the said output signal which is dependent on the phase difference, and

- an oscillator, which is controlled with the aid of the said control word,

wherein

the said controllers also include setting components for setting the measured phase difference as a setting value for the normal adjustment function of the phase lock.

6. (Amended) Arrangement as defined in Claim 4, which includes starting components for starting the normal adjustment function of the loop,

wherein the said starting components respond to the setting components in order to start the adjustment function in response to the setting of a setting value.

REMARKS

The above preliminary amendment is made to insert an abstract page into the application and to amend claims 1-6

Applicant respectfully requests that this preliminary amendment be entered into the record prior to calculation of the filing fee and prior to examination and consideration of the above-identified application.

If a telephone conference would be helpful in resolving any issues concerning this communication, please contact Applicant's attorney of record, Michael B. Lasky at 952-912-0527.

Respectfully submitted,

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Date: December 12, 2001 By: _____

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Appendix A
Marked Up Version of Entire Claim Set

1. (Amended) Method for controlling a phase locked loop during change of synchronisation source, in which method

- the synchronisation signal is changed from a first synchronisation to a second synchronisation signal,

- the phase difference between the said second synchronisation signal [(P1)]and a signal [(P2)] formed from the phase lock's oscillator is measured,

- the phase difference between the second synchronisation signal and the signal formed from the phase lock's oscillator is changed, if the measured phase difference is greater than a predetermined limit value, whereupon the phase difference between the said second synchronisation signal and the signal formed from the phase lock's oscillator is again measured,

- the phase locked loop's normal adjustment function is started, when the measured phase difference is less than or equal to the said limit value,

[c h a r a c t e r i z e d in that] wherein

in response to the finding, that the said phase difference is less than or equal to the said limit value, the measured phase difference is set as the setting value for the phase difference for the normal adjustment function of the phase locked loop, whereupon the adjustment function is started.

2. (Amended) Method as defined in Claim 1, [c h a r a c t e r i z e d in that] wherein phase transfer of the second synchronisation signal is carried out by preventing for a certain time access of the signal formed from the phase lock's oscillator to the component measuring the phase difference of the phase locked loop.

3. (Amended) Method as defined in Claim 2, [c h a r a c t e r i z e d in that] wherein preventing takes place by cutting off the functional route of the signal formed from the oscillator to the component measuring the phase difference of the phase locked loop.

4. (Amended) Method as defined in Claim 2, [c h a r a c t e r i z e d in that] wherein preventing takes place by cutting off the functional route of the second synchronisation signal to the component measuring the phase difference of the phase locked loop.

5. (Amended) Digital phase lock arrangement, which includes,

- selection components [(12,14)] for selecting the desired synchronisation source from a set of at least two different synchronisation sources,

- a phase comparator [(13)], which has a first and a second input and which is used for generating an output signal dependent on the phase difference between the signals supplied to the inputs,

- controllers [(14)] for forming a control word in response to the said output signal which is dependent on the phase difference, and

- an oscillator [(16)], which is controlled with the aid of the said control word,

[c h a r a c t e r i z e d in that] wherein

the said controllers (14) also include setting components for setting the measured phase difference as a setting value for the normal adjustment function of the phase lock.

6. (Amended) Arrangement as defined in Claim 4, which includes starting components for starting the normal adjustment function of the loop,

[c h a r a c t e r i z e d in that] wherein the said starting components respond to the setting components in order to start the adjustment function in response to the setting of a setting value.